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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,246	01/19/2001	Paul Garnett	5181-80100	8288

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EXAMINER	
DANG, KHANH NMN	

ART UNIT	PAPER NUMBER
2111	

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12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/766,246	GARNETT, PAUL	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The drawings are objected to because the blocks in Figs. 3, 4, 6, and 7 have not been labelled. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-37 are rejected under 35 U.S.C. 102(b) as being anticipated by GB 2290891 (Kobayashi et al.)

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted and as best the examiner can ascertain, these claims do not positively define any structure/step that differs from GB 2290891 (891). With regard to claim 21, 27-31, 891 discloses a computer system comprising a plurality of processing sets, each having at least one processor (CPU 5a-5d having a 2-bit ID register provided at each CPU 5a-5d), and a bridge (6) coupled to each of processing sets (1-N) and operable to monitor a step locked operation of processing sets (5 (a-d)), wherein each

of the processors has a processor identification register (2-bit ID register provided at each CPU 5a-5d) which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register (2-bit ID register provided at each CPU 5a-5d). With regard to claims 22 and 23, see the condition of "reset" and "initialization" in 891. With regard to claims 24 and 25, the "initialisation program" stored in ROM 13 is readable as the so-called "boot memory unit." With regard to claim 6, it is clear that the in 891, all register contents can be initialized to zeros by reset signal line 35, for example. With regard to claims 22-25, one using the device of 891 would have performed the same steps set forth in claims 22-25. See also "fault" condition described in detail in 891, that causes error condition. With regard to claims 26 and 27, it is clear that in 891, any processing set (5(a-d)) can be removed and replaced by another processing set, not necessarily identical to the removed one.

Response to Arguments

Applicant's arguments filed 3/25/2004 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of

police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The Klug et al. Rejection:

The Klug et al. rejection is hereby withdrawn in view of Applicant's argument and upon further review of the Klug et al. reference.

The Kobayashi et al. Rejection:

With regard to claim 21 (with claims 22-29 and 32-35 stand or fall together), Applicant argued that Kobayashi et al. does disclose "each of said processor comprises a processor identification register which is read/writable and is configured to store in said register data representative of a processor identification, each of said processors being configured, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor

identification register." Contrary to Applicant's argument, Kobayashi et al.discloses a computer system comprising a plurality of processing sets, each having at least one processor (CPU 5a-5d having a 2-bit ID register provided at each CPU 5a-5d), and a bridge (6) coupled to each of processing sets (1-N) and operable to monitor a step locked operation of processing sets (5 (a-d)), wherein each of the processors has a processor identification register (2-bit ID register provided at each CPU 5a-5d) which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register (2-bit ID register provided at each CPU 5a-5d). It is also clear that under reset condition, a predetermined data value (zero, for example), common to processing sets (all zeros), for example, is loaded into the processor identification register (2-bit ID register provided at each CPU 5a-5d). See at least Fig. 3 and description thereof.

With regard to Applicant's arguments regarding claim 30 (with claims 31, 36, and 37 stand or falls together), see above. In addition, under the reset condition in Kobayashi et al., the predetermined data value (zeros, for example) loaded into the register is operable to mask the data representative of the processor identification.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner